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Attorney Docket No.	*Total Pages :*
2000 1645A	

First Named Inventor or Application Identifier

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Express Mail Label No.:

APPLICATION ELEMENTS

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- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

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Filed November 28, 2000 : Attorney Docket No. 2000_1645A

SEMICONDUCTOR PACKAGE AND
METHOD FOR FORMING
SEMICONDUCTOR PACKAGE

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Respectfully submitted,

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SPECIFICATION

TITLE OF THE INVENTION

Semiconductor Package And Method For Forming Semiconductor Package

BACKGROUND OF THE INVENTION

The present invention relates to a package for a semiconductor used in electronic equipment and a method for forming the semiconductor package.

A semiconductor is an essential component in forming circuits of electronic equipment and, various forms for mounting the semiconductors have been developed and practiced lately. A form of the package as shown in Fig. 12 has been employed to facilitate handling and mounting the semiconductors in the prior art.

An example of the aforementioned prior art will be described with reference to the drawing.

Fig. 12 shows a sectional view of a form of a conventional semiconductor package.

A semiconductor 1 has an upper first electrode (upper a electrode) 2 and an upper second electrode (upper b electrode) 3 set to one face and a lower electrode 5 set to the other entire face. A circuit board 7 has predetermined circuit patterns formed to both faces which are joined by a through hole conductor (not shown), with forming a single

circuit by the two faces. In some cases, balls 8 essentially consisting of gold, silver, copper, or solder are joined, as connecting bodies for connecting the circuit board 7 to another electric circuit, to the circuit pattern of the circuit board 7 to facilitate connection of the circuit board 7 to another electric circuit.

The semiconductor package is formed by joining the semiconductor 1 and the circuit board 7. First, the lower electrode 5 is joined by a solder 6 to the circuit pattern of the circuit board 7. A conductive paste or gold may be used in place of the solder 6 for joining the lower electrode 5 and the circuit pattern.

Meanwhile, the upper first electrode (upper a electrode) 2 and the upper second electrode (upper b electrode) 3 are generally connected to the circuit pattern by wire bonding with use of a gold wire or aluminum wire 4.

In order to protect a circuit forming part primarily consisting of the semiconductor 1, the circuit board 7 at the side of the face to which the semiconductor 1 is mounted is coated with use of an insulating resin 9 in a manner not to deform the joining gold wire or aluminum wire 4. The semiconductor package is formed in this manner with a protection effect and an ease of use improved.

The insulating resin 9 is supplied by molding with use of a mold, pouring the molten resin or, heating and

melting the resin of powder or particles after placing the resin on an upper face of the semiconductor 1 thereby coating the semiconductor entirely, or the like manner.

When the semiconductor heats by a larger amount in the above-described constitution, the circuit board is not enough to radiate heat. Even if the circuit board is formed of ceramic of a good heat conductivity and used to radiate heat to a heat radiating plate or the like, emphasis is put on forming the circuit pattern, that is, heat radiation is less taken into consideration, whereby a radiation loss is easy to generate. Also, even if the gold wire or aluminum wire is utilized to radiate heat, since the gold wire or aluminum wire used for wire bonding is limited in diameter, the wire should be used within a current capacity allowed for its diameter. A plurality of joints must be carried out to one electrode to cope with a large current as in a power source circuit. Although a distance between electrodes must be secured to ensure safety and reliability in accordance with a current increase, the distance is hard to secure in the case of the gold wire or aluminum wire because the wire is varied in shape at the time of wire bonding or deformed during processes afterwards, or the like.

SUMMARY OF THE INVENTION

The object of the present invention is accordingly to remove the above issue and provide a semiconductor

package which is comprised of one or a plurality of semiconductors and can exert a superior heat radiation effect in a simple structure and a stable quality and, a method for forming the semiconductor package.

In order to accomplish the above objective, the present invention is constituted as will be described below.

In accomplishing these and other aspects, according to a first aspect of the present invention, there is provided a semiconductor package comprising:

a first semiconductor having electrodes formed to both of an upper and a lower faces;

a heat radiating plate to which a lower face electrode of the first semiconductor is joined with use of a joining member; and

pillared or spherical electrodes which are joined to the upper face electrodes of the first semiconductor and the heat radiating plate respectively.

According to a second aspect of the present invention, there is provided a semiconductor package according to the first aspect, further comprising a sealing resin with which the first semiconductor and a face of the heat radiating plate joined to the first semiconductor are covered in a manner to expose a part of leading ends of the pillared or spherical electrodes.

According to a third aspect of the present

invention, there is provided a semiconductor package according to the first or second aspect, further comprising a second semiconductor having electrodes formed to both of an upper and a lower faces and of the same kind of the first semiconductor, a lower face electrode of the second semiconductor being joined to the heat radiating plate with use of a joining member, the heat radiating plate having an electric circuit of an equal polarity formed of a single or a combination material of gold, silver, copper, nickel, and tungsten and set to ceramic, with the first and second semiconductors being joined to the electric circuit of the equal polarity.

According to a fourth aspect of the present invention, there is provided a semiconductor package according to the first or second aspect, further comprising a third semiconductor having electrodes formed to both of an upper and a lower faces and of a different kind of the first semiconductor, a lower face electrode of the third semiconductor being joined to the heat radiating plate with use of a joining member, the heat radiating plate having an electric circuit of a plurality of polarities independently with the circuit being formed of a single or a combination material of gold, silver, copper, nickel, and tungsten and set to ceramic and with the first and third semiconductors of the different kinds being joined respectively to the

plurality of polarities of the electric circuit.

According to a fifth aspect of the present invention, there is provided a semiconductor package according to any one of the first through fourth aspects, wherein the heat radiating plate is constituted of ceramic in a multilayer structure, having a circuit for the semiconductor and the pillared or spherical electrodes with the circuit being formed of a single or a combination material of gold, silver, copper, nickel, and tungsten and set to a front face thereof, and the heat radiating plate has conductor layers formed of an equal material to a material of the electrodes of the front face thereof and arranged between layers of the ceramic to be connected to the circuit of the front face, so that heat of the semiconductor is radiated by both the ceramic and the conductor layers.

According to a sixth aspect of the present invention, there is provided a semiconductor package according to the first or second aspect, wherein the heat radiating plate is formed of any one material of copper, copper alloy, aluminum, and aluminum alloy, or any one of the metals subjected to surface treatment.

According to a seventh aspect of the present invention, there is provided a semiconductor package according to any one of the first, second through sixth

aspects, wherein a sealing resin and the pillared or spherical electrodes are formed by removing simultaneously part of the sealing resin and part of the pillared or spherical electrodes after the pillared or spherical electrodes are covered with the sealing resin, thereby exposing the pillared or spherical electrodes to constitute electric connecting parts.

According to an eighth aspect of the present invention, there is provided a semiconductor package according to any one of the first through seventh aspects, wherein the pillared or spherical electrodes have leading ends pressed smoothly to a uniform height.

According to a ninth aspect of the present invention, there is provided a semiconductor package according to any one of the first through eighth aspects, wherein the pillared or spherical electrode is formed of materials of different hardnesses between an inside thereof and an outside thereof.

According to a 10th aspect of the present invention, there is provided a semiconductor package according to any one of the first through eighth aspects, wherein the pillared or spherical electrode is formed of materials of different melting temperatures between an inside thereof and an outside thereof.

According to an 11th aspect of the present

invention, there is provided a semiconductor package according to any one of the first through third aspects, wherein further comprising a fourth semiconductor having electrodes formed to both of an upper and a lower faces and of a different kind of the first semiconductor and having a lower face electrode of an equal current and voltage characteristics to the first semiconductor, the lower face electrode of the fourth semiconductor being joined to the heat radiating plate with use of a joining member, the first and fourth semiconductors are mounted on the heat radiating plate.

According to a 12th aspect of the present invention, there is provided a semiconductor package according to any one of the first through 11th aspects, wherein the heat radiating plate is provided with pits and projections to a front face of a face opposite to a face joined to the semiconductors.

According to a 13th aspect of the present invention, there is provided a semiconductor package according to any one of the first through 12th aspects, wherein a plurality of bumps are disposed between the upper face electrodes of the semiconductor and the pillared or spherical electrodes.

According to a 14th aspect of the present invention, there is provided a method for forming a

semiconductor package, comprising:

joining a lower face electrode of a first semiconductor which has electrodes formed to both of an upper and a lower faces to a heat radiating plate with use of a joining member; and

joining pillared or spherical electrodes to the upper face electrodes of the first semiconductor and the heat radiating plate respectively.

According to a 15th aspect of the present invention, there is provided a method for forming a semiconductor package according to the 14th aspect, further comprising, after the pillared or spherical electrodes are respectively joined to the upper face electrodes of the first semiconductor and the heat radiating plate, covering the first semiconductor and a face of the heat radiating plate joined to the first semiconductor with a sealing resin in a manner to expose a part of leading ends of the pillared or spherical electrodes.

According to a 16th aspect of the present invention, there is provided a method for forming a semiconductor package according to the 14th or 15th aspect, wherein when the first semiconductor is joined to the heat radiating plate, a lower face electrode of a second semiconductor of the same kind of the first semiconductor which has electrodes formed to both of an upper and a lower

faces is joined to the heat radiating plate with use of a joining member and the first and second semiconductors are joined to an electric circuit of an equal polarity of the heat radiating plate with the electric circuit of the equal polarity being formed of a single or a combination material of gold, silver, copper, nickel, and tungsten and set to ceramic.

According to a 17th aspect of the present invention, there is provided a method for forming a semiconductor package according to the 14th or 15th aspect, wherein when the first semiconductor is joined to the heat radiating plate, a lower face electrode of a third semiconductor of a different kind of the first semiconductor which has electrodes formed to both of an upper and a lower faces is joined to the heat radiating plate with use of a joining member and the first and third semiconductors are joined to an electric circuit of a plurality of polarities independently of the heat radiating plate with the electric circuit being formed of a single or a combination material of gold, silver, copper, nickel, and tungsten and set to ceramic.

According to an 18th aspect of the present invention, there is provided a method for forming a semiconductor package according to any one of the 14th through 17th aspects, further comprising, before the

semiconductor is joined to the heat radiating plate, forming, on a front face of the heat radiating plate constituted of ceramic in a layer structure, a circuit for the semiconductors and the pillared or spherical electrodes by a single or a combination material of gold, silver, copper, nickel, and tungsten, and arranging conductor layers of an equal material to a material of the electrodes of the front face between layers of the ceramic to be connected to the circuits of the front face thereof, so that heat of the semiconductors is radiated by both the ceramic and the conductor layers.

According to a 19th aspect of the present invention, there is provided a method for forming a semiconductor package according to the 14th or 16th aspect, wherein, before the semiconductor is joined to the heat radiating plate, forming the heat radiating plate by any one material of copper, copper alloy, aluminum, and aluminum alloy, or any one of the metals subjected to surface treatment.

According to a 20th aspect of the present invention, there is provided a method for forming a semiconductor package according to any one of the 14th through 19th aspects, further comprising:

after the pillared or spherical electrodes are respectively joined to the upper face electrodes of the

first semiconductor and the heat radiating plate, covering the pillared or spherical electrodes with the sealing resin; and

thereafter removing part of the sealing resin and part of the pillared or spherical electrodes simultaneously, thereby exposing the pillared or spherical electrodes to constitute electric connecting parts.

According to a 21st aspect of the present invention, there is provided a method for forming a semiconductor package according to any one of the 14th through 20th aspects, further comprising, after the pillared or spherical electrodes are respectively joined to the upper face electrodes of the first semiconductor and the heat radiating plate, pressing smoothly leading ends of the pillared or spherical electrodes to a uniform height.

According to a 22nd aspect of the present invention, there is provided a method for forming a semiconductor package according to any one of the 14th through 21st aspects, wherein when the pillared or spherical electrodes are respectively joined to the upper face electrodes of the first semiconductor and the heat radiating plate, the pillared or spherical electrode formed of materials of different hardnesses between an inside thereof and an outside thereof is used.

According to a 23rd aspect of the present

invention, there is provided a method for forming a semiconductor package according to any one of the 14th through 21st aspects, wherein when the pillared or spherical electrodes are respectively joined to the upper face electrodes of the first semiconductor and the heat radiating plate, the pillared or spherical electrode formed of materials of different melting temperatures between an inside thereof and an outside thereof is used.

According to a 24th aspect of the present invention, there is provided a method for forming a semiconductor package according to any one of the 14th through 16th aspects, wherein when the first semiconductor is joined to the heat radiating plate, a lower face electrode of a fourth semiconductor having electrodes formed to both of an upper and a lower faces and of a different kind of the first semiconductor and having the lower face electrode of an equal current and voltage characteristics to the first semiconductor, is joined to the heat radiating plate with use of a joining member, so that the first and fourth semiconductors are mounted on the heat radiating plate.

According to a 25th aspect of the present invention, there is provided a method for forming a semiconductor package according to any one of the 14th through 24th aspects, further comprising providing the heat

radiating plate with pits and projections at a front face of a face opposite to the face joined to the semiconductors.

According to a 26th aspect of the present invention, there is provided a method for forming a semiconductor package according to any one of the 14th through 25th aspects, further comprising forming a plurality of bumps to the upper electrodes of the semiconductors,

wherein when the pillared or spherical electrodes are joined to the upper face electrodes of the semiconductor, the pillared or spherical electrodes are joined to the upper face electrodes of the semiconductor via the plurality of bumps.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects and features of the present invention will become clear from the following description taken in conjunction with the preferred embodiments thereof with reference to the accompanying drawings, in which:

Fig. 1 is a plan view of a semiconductor package according to a first embodiment of the present invention;

Fig. 2 is a sectional view of the semiconductor package of the first embodiment of the present invention taken along a line A-A of Fig. 1;

Fig. 3 is a sectional view of a semiconductor package according to a second embodiment of the present

invention;

Fig. 4 is a plan view of a semiconductor package according to a third embodiment of the present invention;

Fig. 5 is a sectional view of the semiconductor package of the third embodiment of the present invention taken along a line B-B of Fig. 4;

Fig. 6 is a sectional view of a semiconductor package according to a fourth embodiment of the present invention assumed to be cut along a line B-B' of Fig. 4;

Figs. 7A and 7B are sectional views of a semiconductor package according to a sixth embodiment of the present invention;

Figs. 8A and 8B are sectional views of a semiconductor package according to a seventh embodiment of the present invention;

Figs. 9A, 9B, and 9C are sectional views of a semiconductor package according to an eighth embodiment of the present invention;

Fig. 10 is a sectional view of a semiconductor package according to a ninth embodiment of the present invention;

Figs. 11A and 11B are a plan view and a sectional view of a semiconductor package according to a 10th embodiment of the present invention;

Fig. 12 is a sectional view of a semiconductor

package of the prior art;

Fig. 13 is a plan view of the semiconductor package in the third embodiment of the present invention when electric circuits of an equal polarity are formed to a whole surface of a ceramic radiating plate;

Fig. 14 is a sectional view showing a state of joining a circuit board and a semiconductor element with use of the semiconductor package of the eighth embodiment of the present invention;

Fig. 15 is a sectional view of a state of joining a circuit board and a semiconductor element with use of the semiconductor package of the eighth embodiment of the present invention; and

Figs. 16, 17, and 18 are sectional views of semiconductor packages according to other examples of the eighth embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before the description of the present invention proceeds, it is to be noted that like parts are designated by like reference numerals throughout the accompanying drawings.

Semiconductor packages and methods for forming the semiconductor packages according to embodiments of the present invention will be discussed in detail below on the basis of drawings.

(FIRST EMBODIMENT)

Fig. 1 is a plan view of a semiconductor package according to a first embodiment of the present invention, and Fig. 2 is a sectional view of the semiconductor package.

In the semiconductor package according to the first embodiment of the present invention, the lower face electrode of a semiconductor 1 has electrodes formed to both upper and lower faces, and the lower face electrode of the semiconductor 1 is joined to a heat radiating plate 10 with use of a solder, and the upper face electrodes 2 and 3 of the semiconductor 1 and the radiating plate 10 are joined to pillared or spherical electrodes 11.

The metallic heat radiating plate 10 is formed of any one of copper, copper alloy, aluminum, and aluminum alloy. The metallic radiating plate 10 and the lower electrode (lower face electrode) of the semiconductor 1 having the electrodes to the upper and lower both faces are joined with each other by the solder. A thickness of a layer formed of the solder is made as small as possible, so that its heat conduction efficiency is improved. Other examples of the joining member are conductive paste, gold, or the like. When the joining member is solder, heat conductance, joining properties (easiness of joining) to the semiconductor, and heat resistance may be improved. When the embodiment is applied to drivers of industrial motors

such as AC servo motors and there is caused any lock of the rotation of the motor to generate heat of about 120°C to which the joining member is subjected, such a joining member is preferably formed of solder. When the joining member is of gold, the heat conduction properties become high and the electrical resistance becomes lower.

The pillared or spherical electrodes 11 formed of a metal essentially consisting of any one of gold, silver, copper, and aluminum are joined to the upper first electrode (upper a) electrode 2 and the upper second electrode (upper b electrode) 3 of the semiconductor 1 and to the metallic radiating plate 10 with use of ultrasonic oscillation, solder, or conductive paste. The conductive paste is a mixture of a metallic powder such as gold, silver, or the like and generally an epoxy resin or silicone resin having thermosetting properties and insulating properties, thereby exhibiting electric conductive and adhesive properties.

Leading end parts of the pillared or spherical electrodes 11 at the side not to be joined to the semiconductor 1 and the metallic radiating plate 10 are used for joining to a circuit board after the semiconductor package is completed. For this purpose, it is necessary to form the pillared or spherical electrodes 11 without a step, in other words, at an approximately equal height.

Mixed-mounting of semiconductors 1 of different

kinds can be carried out on the metallic radiating plate 10 if the semiconductors have equal current and voltage characteristics related to the lower electrodes.

In the above constitution, the lower electrode of the semiconductor 1 is joined to the radiating plate 10 with use of the solder, while the upper electrodes (upper face electrodes) 2 and 3 of the semiconductor 1 and the radiating plate 10 are joined to the pillared or spherical electrodes 11. When the radiating plate 10 of the metal is used, the semiconductor 1 is always joined directly only via the solder to the metallic radiating plate 10, so that the heat of the semiconductor 1 is considerably quickly transmitted to the metallic radiating plate 10, spread in the whole of the radiating plate 10 and radiated from a surface of the radiating plate 10. A temperature rise of the semiconductor 1 is accordingly prevented. Moreover, the metallic radiating plate 10 is utilizable as a conductor for the lower electrode if a connecting terminal is joined to the radiating plate 10.

(SECOND EMBODIMENT)

Fig. 3 is a sectional view of a semiconductor package according to a second embodiment of the present invention which uses a sealing resin 12 having insulating property.

The semiconductor package in the second embodiment

of the present invention is formed by covering the semiconductor package of the first embodiment with the sealing resin 12 in a manner to partly expose the pillared or spherical electrodes 11.

More specifically, after joining the pillared or spherical electrodes 11 of the first embodiment, the semiconductor 1 is covered with the sealing resin 12 with use of a mold or jig so that end parts of the pillared or spherical electrodes 11 at the side joined to the circuit board project, e.g., by approximately 50-200μm thereby forming projecting parts 13.

When the mold is to be used, the semiconductor package of the first embodiment is arranged beforehand within a cavity of the mold. The molten sealing resin 12 is injected into the cavity generally by injection molding, then cooled and hardened. When the jig is to be used, on the other hand, the metallic radiating plate 10 is surrounded in the periphery by a material not joined to the sealing resin 12, and then the molten sealing resin 12 is poured therein, cooled and hardened. Alternatively, a specified amount of the powder or particle sealing resin 12 is put in the periphery, heated, melted, cooled and hardened.

In the above-described arrangement, after the lower face electrode of the semiconductor 1 having the electrodes to the upper and lower faces is joined to the

radiating plate 10 with use of the solder and, the upper electrodes 2 and 3 of the semiconductor 1 and the radiating plate 10 are joined to the pillared or spherical electrodes 11, the semiconductor 1 is covered with the sealing resin 12 to expose the projecting parts 13 as part of the pillared or spherical electrodes 11. Since the semiconductor 1 is covered with the sealing resin 12 except leading end parts 13 of the pillared or spherical electrodes 11, each component is protected from deformation, damage, moisture, dust, or the like and the semiconductor package after completed becomes easy to handle.

(THIRD EMBODIMENT)

Figs. 4 and 5 are a plan view and a sectional view of a semiconductor package according to a third embodiment of the present invention which uses a ceramic radiating plate 14 having insulating property.

In Figs. 4 and 5, an electrode circuit 15 (15A, 15B) for joining the lower electrode of the semiconductor 1 (1A, 1B) is formed to an upper face of the ceramic radiating plate 14 with use of gold, silver, copper, nickel, tungsten, or the like.

In the case where one semiconductor 1 of the same kind is to be mounted, where a plurality of semiconductors 1 are to be mounted, or where a plurality of semiconductors 1A, 1B of different kinds with equal current and voltage

characteristics at the side of the lower electrodes are to be mounted, the electrode circuit 15 (15A or 15B) of an equal polarity is formed of the aforementioned material to the entire surface of the ceramic radiating plate 14 as shown in Fig. 13.

On the other hand, in the case where a plurality of semiconductors 1A and 1B of different kinds and different current and voltage characteristics at the side of the lower electrodes are to be mounted, electrode circuits 15A and 15B of a plurality of different polarities independently of each other are formed for the respective semiconductors 1A and 1B to set the pillared or spherical electrodes 11 for the lower electrodes, as shown in Fig. 4.

Any of the semiconductors 1, 1A, and 1B is mounted by soldering onto the formed circuit 15, 15A, 15B respectively. Thereafter, the pillared or spherical electrodes 11 are joined onto the semiconductor 1, 1A, 1B and the electrode circuit 15, 15A, 15B with use of any one of ultrasonic oscillation, solder, and conductive paste.

In forming the electrode circuit 15 of a conductive paste, a resin component in the conductive paste is preferably burnt by baking at 600-1600°C to effectuate intermetallic bond, so that the heat conduction efficiency is improved through firm joining of the circuit 15 with the ceramic radiating plate 14.

Generally, when the current and voltage characteristics are different between lower electrodes of semiconductors 1A and 1B of different kinds to be mounted on the same radiating plate 14, the mounting is impossible if the radiating plate is metallic. However, in the arrangement of the third embodiment, the electric circuit 15 of the same polarity, or electric circuits 15A and 15B of a plurality of polarities are formed of a single or a combination material of gold, silver, copper, nickel, or tungsten to the entire face or part of the face of the ceramic radiating plate 14, while the radiating plate 14 and the semiconductor 1, or, 1A and 1B are joined and also the radiating plate 14 and the pillared or spherical electrodes 11 are joined. Since the plurality of polarities are provided independently of each other on the radiating plate 14 with utilization of insulating, heat conductive, and radiation properties of the ceramic, the semiconductors can be independent and mounted on an equal face. At the same time, when the semiconductor is covered with the sealing resin 12 in the application of the earlier second embodiment, since the radiating plate 14 itself is an insulator, electrically active parts except the leading end parts 13 of the pillared or spherical electrodes 11 to be connected to the circuit board are prevented from being exposed, therefore being improved in safety and reliability.

Moreover, a thin wiring is eliminated and an allowable current can be made large when the electric circuit 15 of an equal polarity is formed. An area of a metallic wiring conducting heat well is increased, whereby heat radiation properties can be improved.

(FOURTH EMBODIMENT)

A semiconductor package according to a fourth embodiment of the present invention will be described with reference to Fig. 6. Fig. 6 is a sectional view of a multilayer of ceramic radiating plates 14.

The semiconductor package in the fourth embodiment has a radiating plate 40 formed of ceramic in a layered structure. The semiconductor 1 and electrodes for pillared or spherical electrodes are formed of a single or a combination material of gold, silver, copper, nickel, and tungsten to a front face of the radiating plate 40, and conductor layers to be connected to the electrodes of the front face are formed of an equal material to a material of the electrodes of the front face between the ceramic layers of the radiating plate 40. Heat of the semiconductor 1 is accordingly radiated by both the ceramic layers and the conductor layers.

A method for forming the ceramic of the radiating plate 40 in many layers is not different from generally used ones. For instance, in the case where the radiating plate

40 is constituted of an upper ceramic plate 14a and a lower ceramic plate 4b, holes 16 are formed to the upper ceramic plate 14a and electrode circuit(s) 15C are formed to a front face of the upper ceramic plate 14a. Moreover, an equal material to a material of the electrode circuit(s) 15C is filled in the holes 16, thereby forming conductor layers 15D. In the meantime, electrode circuits of a necessary area are formed as internal conductors 17 to a front face of the lower ceramic plate 14b. Thereafter, the upper ceramic plate 14a and lower ceramic plate 14b are united while the conductor layers 15D of the upper ceramic plate 14a are electrically joined with the internal conductors 17 of the lower ceramic plate 14b, as shown in Fig. 6. The ceramic plate 14a and ceramic plate 14b are united with use of an adhesion force generated in consequence of drying and baking a conductive paste used for forming the electrode circuits 15C, 15D and the internal conductors 17 or use of the other adhesive so that the ceramic plate 14a and ceramic plate 14b are joined to each other. Another method uses a ceramic green sheet, in which the above upper and lower ceramic plates 14a and 14b are replaced with the green sheets. After the same process as above, the ceramic green sheets and conductive paste are simultaneously baked and united at 600-1600°C. The semiconductor 1 and the pillared or spherical electrodes 11 are mounted to the thus-formed

ceramic radiating plate 40, whereby the semiconductor package is completed as indicated in Fig. 6.

In this case, the heat generated at the semiconductor 1 is directly transmitted to the joined electrode circuits 15C and to the internal conductors 17 via the conductor layers 15D inside the holes 16 further to the ceramic plate 14b. The heat is radiated from a lower surface of the lower ceramic plate 14b. Although the radiating plate 40 in the figure is constituted of two ceramic plates 14a and 14b, the ceramic plates can be overlapped in many layers by repeating the same process.

Normally, the transmission of heat is carried out not only via the conductor layers 15D in the holes 16, but through every joined part.

In the arrangement, the radiating plate 40 is constructed in a layered structure of ceramic, with having the semiconductor 1 and the electrodes for pillared or spherical electrodes 11 formed of a single or a combination material of gold, silver, copper, nickel, and tungsten to the front face and having conductor layers 15C, 15D, and 17 formed of the same material as the material of the electrodes of the front face between the ceramic layers to be connected with the electrodes of the front face, so that the heat is radiated both from the ceramic radiating plate 40 and the conductor layers 15C, 15D, and 17. More

specifically, a heat conduction performance of the metal is utilized in order to improve more heat radiation efficiency of the ceramic of the radiating plate 40. In addition, the conductor layers 15D and internal conductors 17 are set as a heat-transmitting metallic layer inside the ceramic of the radiating plate 40 to be connected to the electric circuit(s) 15C of the front face of the radiating plate 40 connected with the semiconductor 1 in order to transmit the heat generated at the semiconductor 1 as fast as possible to the whole of the radiating plate 40. The heat can thus be transmitted from the electric circuit(s) 15C through the conductor layers 15D and the internal conductors 17 to the lower ceramic plate 14b. A heat diffusion efficiency can be improved and the heat radiation efficiency can be made further better.

(FIFTH EMBODIMENT)

In a semiconductor package according to a fifth embodiment of the present invention, the radiating plate is formed of any single material of copper, copper alloy, aluminum, and aluminum alloy, or the one metal thereof after subjected to surface treatment. Since the copper, copper alloy, aluminum, or aluminum alloy has a good processability to allow various working methods of cutting, casting, and the like, a large degree of freedom in shape is effectuated and a use range is enlarged in combination with the surface

treatment.

As above, when the radiating plate is formed of any one material of copper, copper alloy, aluminum, and aluminum alloy or the one metal thereof after subjected to the surface treatment, if one semiconductor 1 is to be mounted or a plurality of semiconductors 1 including lower electrodes of an equal current and voltage characteristics are to be mounted, the radiating plate itself may be a conductor. Since the above material transmits heat and electricity good, diffuses heat fast, and is easy to solder among metals, the heat of the semiconductor 1 can be radiated more effectively.

(SIXTH EMBODIMENT)

A semiconductor package in a sixth embodiment of the present invention will be described with reference to Figs. 7A and 7B.

The semiconductor package in the sixth embodiment of the present invention is obtained by covering pillared or spherical electrodes 11 with the sealing resin 12 as shown in Fig. 7A, then simultaneously removing part of the sealing resin 12 and part of the pillared or spherical electrodes 11 to expose electrode parts of the pillared or spherical electrodes 11, thereby forming connecting parts as shown in Fig. 7B.

More specifically, in Fig. 7A, the semiconductor 1

and the pillared or spherical electrodes 11 mounted on an electrode circuit of the metallic radiating plate 10 or ceramic radiating plate 14 are covered with the sealing resin 12 with use of a mold or a jig as described in the second embodiment. The sealing resin 12 is applied by an amount at least covering leading end parts of the pillared or spherical electrodes 11, preferably, an amount whereby a margin is provided to the leading end parts as indicated in Fig. 7A. Thereafter, in Fig. 7B, a part 18, that is, an upper part of the pillared or spherical electrodes 11 and part of the sealing resin 12 formed in Fig. 7A is removed, whereby a smooth face 19 is formed and end faces of the pillared or spherical electrodes 11 are exposed.

The part 18 is removed by cutting by means of a rotating or reciprocating cutting tool or rotating an abrasive paper.

The removal is carried out on the basis of a lower face of the metallic radiating plate 10 or ceramic radiating plate 14, whereby a total height is uniformed without the need of carefully taking the amount of the sealing resin 12 into account.

According to this constitution, part of the sealing resin 12 and part of the pillared or spherical electrodes 11 are removed at the same time after the pillared or spherical electrodes 11 are covered with the

sealing resin 12, thereby exposing the electrode parts of the pillared or spherical electrodes 11 to form the connecting parts. Electrodes are accurately uniformed in height. In other words, although it is considerably difficult to uniform a plurality of electrodes 11 in height when the pillared or spherical electrodes 11 are set on the electrode circuit of the semiconductors 1 and the metallic radiating plate 10 or ceramic radiating plate 14, all the electrodes 11 can be uniformed in height by removing part of all electrodes 11 together with part of the sealing resin 12, so that an accuracy necessary for mounting can be fully satisfied.

(SEVENTH EMBODIMENT)

A semiconductor package according to a seventh embodiment of the present invention will be discussed with reference to Figs. 8A and 8B. The semiconductor package of the seventh embodiment of the present invention has pillared or spherical electrodes 11 joined to the semiconductors 1 and a metallic radiating plate 10 or sealed with the sealing resin 12, and pressed smoothly thereafter.

The pillared or spherical electrodes 11 joined to the semiconductors 1 and the metallic radiating plate 10 or ceramic radiating plate 14 are not always constant in height because of working errors of individual parts to be joined to each other and processing errors at the time of joining

the parts. However, the pillared or spherical electrodes 11 are preferably uniform in height as much as possible to mount to the circuit board. Therefore, leading end parts of the pillared or spherical electrodes 11 are pressed to be deformed by a smoothing plate 20 having a smooth face, thereby uniforming the height. Fig. 8A is a diagram of a state in which the electrodes are pressed in the absence of the sealing resin 12, whereby a pressure of the pressing is directly transmitted to joined parts with the semiconductors 1 because of no sealing resin 12. As such, the pressing force should be determined with a break of the semiconductors 1 being taken into consideration.

In Fig. 8B, the pillared or spherical electrodes 11 are covered with the sealing resin 12 in a manner to expose leading end parts of the electrodes 11 with use of the method in the above-described second embodiment or the like. The pillared or spherical electrodes 11 are pressed by the smoothing plate 20 and deformed at the exposed parts, thereby being uniformed in height. In this case, a large pressing force is required because the pillared or spherical electrodes 11 include only a small part that can be deformed. However, the pressing force is supported by the sealing resin 12 and scattered. The pressing force is prevented from being directly transmitted to the semiconductors 1. The semiconductors 1 are accordingly less damaged in

comparison with Fig. 8A. An allowance for a set value of the pressing force can be made large as compared with Fig. 8A and a workability is improved.

According to the above construction, the smooth pressing is conducted after the pillared or spherical electrodes 11 are joined to the semiconductors 1 and the metallic radiating plate 10 or ceramic radiating plate 14 or sealed with the sealing resin 12. The constitution of the embodiment can exert the same effects as the sixth embodiment. The pillared or spherical electrodes 11 can be easily uniformed in height by deforming the electrodes 11 through pressing with use of a jig or a mold having a smooth face.

(EIGHTH EMBODIMENT)

A semiconductor package according to an eighth embodiment of the present invention will be described with reference to Figs. 9A, 9B, and 9C which are sectional views of a pillared electrode 11 by way of example of the pillared or spherical electrode 11 in the eighth embodiment of the present invention.

In the eighth embodiment, the pillared electrode 11 is formed in a double structure of different materials. A material constituting an inside and a material constituting an outside are different in hardness.

The pillared electrode 11 in a first example of

the eighth embodiment is in the double structure as shown in Fig. 9A, having a hard inside and a soft outside, or as shown in Figs. 16-18, having the outside formed of a material of a lower melting temperature than the inside. More specifically, Fig. 9A shows the pillared electrode 11 in section which is formed of an inner member 21 and an outer member 22. The inner member 21 is obtained by cutting a wire or bar stock of copper or a copper alloy to a constant size and finishing a surface smoothly by barrel finishing or the like. The outer member 22 is obtained by plating a material softer than copper, i.e., solder, tin, an alloy of tin and bismuth, or an alloy of tin and lead to a front face of the inner member 21. A plating thickness of the outer member 22 is, e.g., approximately 20-100μm. When the electrode is pressed in an arrow direction in Fig. 9B at the time of joining to the substrate, an upper and a lower soft plated parts of the outer member 22 are deformed as illustrated in Figs. 9B and 14, whereas a hard part of the inner member 21 is not deformed. The whole of the pillared electrode 11 is prevented from being largely deformed and maintains its shape. In Fig. 14, 42 is a base material and 41 is a copper electrode, which constitute the circuit board 5. Metal diffusion is brought about to a part where the outer member 22 and the copper electrode 41 are in contact with each other and a part where the outer member 22 and the

aluminum electrode 2 or 3 are in contact with each other. In the constitution of the electrode, a height of the electrode can be determined accurately and a high rigidity can be secured. The plating thickness of the outer member 22 is set to be not smaller than 20μm because this is a minimum value (minimum value from experiments) whereat the plated part is started to be deformed and a minimum value necessary for absorbing the height variation. The plating thickness of not larger than 100μm of the outer member 22 is set because the value is generally considered as a maximum plating thickness.

Figs. 16-18 show the pillared electrodes 11 in section each of which is formed of an inner member 21A and an outer member 22B. The inner member 21A is obtained by cutting a wire or bar stock of copper (melting point (melting temperature) of 1084.5°C), aluminum (melting point of 660.4°C), or gold(melting point of 1064.43°C) to a constant size and finishing a surface smoothly by barrel finishing or the like. The outer member 22B is obtained by plating solder (melting point of 180-300°C) such as Sn-Ag-Cu-based, Sn-Cu-based, Sn-Au-based, Sn-Bi-based, or Sn-Pb-based solder, as a material having a melting point lower than that of the inner member 21A, to a front face of the inner member 21A. Because of the solder of the outer member 22B, the joining strength can be more improved. Even in

this case, similar to Fig. 9A, when the electrode is pressed in the arrow direction in Fig. 9B at the time of joining to the substrate, an upper and a lower plated parts of the outer member 22B are deformed as similar to Figs. 9B and 14, whereas the inner member 21A is not deformed. The whole of the pillared electrode 11 is prevented from being largely deformed and maintains its shape. A dotted line in Fig. 18 shows an electrode of a circuit board.

In the meantime, in a second example of the eighth embodiment, materials are switched between the inner member 21 and outer member 22, that is, the inner member 21 is formed of a wire or rod stock softer than copper, namely, any one of tin, tin-bismuth alloy, and tin-lead alloy which is cut to a constant size and finished smoothly at a front face by barrel finishing or the like manner. Then, a plated layer of a material harder than the material of the inner member 21, i.e., copper or copper alloy is formed as the outer member 22 at the surface of the inner member 21 in a thickness of approximately 3-50μm by plating. The outer member 22 is prevented from being broken when pressured in an arrow direction of Fig. 9C and, eventually deformed as shown in Figs. 9C and 15. 42 and 41 in Fig. 15 are respectively a base material and a copper electrode which constitute the circuit board 5. Metal diffusion is brought about to a contact part between the outer member 22 and the

copper electrode 41 and a contact part between the outer member 22 and the aluminum electrode 2 or 3. According to the constitution, an irregularity in height of the circuit board can be absorbed and also a uniform pressure is applied to electrodes through the deformation even when a plurality of electrodes are pressed at one time at the joining time. Different from the foregoing example, the plating thickness of the outer member 22 is set to be not smaller than 3μm, because the inner member 21 is deformed thereby eliminating the need of deforming the outer member 22. The metal diffusion can be generated good by having the thickness not smaller than 3μm without breaking the outer member. At the same time, the thickness of not larger than 50μm is set because the value approximately half of the plating thickness 100μm of the outer member 22 is considered appropriate.

When the pillared electrode 11 is constituted as in the above first example or second example, the electrode is hard to deform during the joining or the like whereas the electrode is easy to deform when a height adjustment is required. Excessive pressing is thus not required to adjust the height by the smoothing plate 20 with the application of the seventh embodiment, so that the damage to the semiconductors 1 is eliminated. Furthermore, the work by the smoothing plate 20 is eliminated and the electrode can

be deformed with a small amount of pressing when mounted to the circuit board. The height can be adjusted with an error at the side of the circuit board being absorbed.

To any deformation of the pillared electrodes 11 of the first example and second example, the height adjustment can be by approximately 5-30μm.

As described hereinabove, according to the first example of the eighth embodiment, the pillared or spherical electrode 11 is in the double structure of the soft inside and hard outside or in the double structure having the outside formed of the material of a lower melting temperature than the inside. In the pillared or spherical electrodes 11 comprised of the inside of copper or copper alloy and the outside of a soft material of any of tin, tin-bismuth alloy, and tin-lead alloy, the soft outer member 22 is deformed at the time of joining to the circuit board, whereas the inner member 21 is supported by the hard copper or copper alloy. The pillared or spherical electrodes 11 show no great deformation as a whole, with a smoothness secured at the leading end parts thereof.

The smoothness can be secured by adjusting the height through smoothly pressing and deforming the electrodes in a heightwise direction, thereby coping with a height irregularity of the electrodes at the side of the circuit board when the electrodes are mounted as a

semiconductor package to the circuit board, in other words, absorbing the height irregularity of the electrodes on the circuit board.

According to the second example of the eighth embodiment, the pillared or spherical electrode 11 is in the double structure of the soft inside and hard outside, or in the double structure having the outside of the material of a higher melting temperature than the inside. The same effect as in the first example can be obtained even by switching the materials between the inside and outside of the pillared or spherical electrode 11.

(NINTH EMBODIMENT)

A semiconductor package according to a ninth embodiment of the present invention will be described with reference to Fig. 10. In the ninth embodiment of the present invention, pits and projections are formed to a front face of an opposite face of the radiating plate to the face joined to the semiconductor so as to increase the surface are thereof resulting in improving the heat radiation effect.

In any radiating plate of the metallic radiating plate 10 and the ceramic radiating plates 14, 40, pits and projections 23 are formed to the front face of the face opposite (lower face in Fig. 10) to the face (upper face in Fig. 10) where the pillared or spherical electrodes 11 are

mounted to the semiconductors 1, 1A, 1B. Because of the presence of the pits and projections 23 at the front face, a surface area is increased and a contact area with the air is increased, so that a heat radiation effect is improved. That is, the instantaneously generated heat of the semiconductors 1, 1A, 1B is absorbed by a part of a large volume density without the pits and projections 23 (namely, the face of the radiating plate where the semiconductors are mounted). Then the heat is conducted and transmitted to the pits and projections 23 and radiated from the surface of the pits and projections 23. Although a sectional shape of the pits and projections 23 is illustrated nearly triangular in Fig. 10, the shape is not limited particularly to the triangle and can be rectangle, corrugated from, or other forms.

When the pits and projections 23 are formed to the front face of the face opposite to the face of the radiating plate 10, 14, 40 where the semiconductors 1, 1A, 1B are joined in the construction, the surface area of the radiating plate 10, 14, 40 is increased, so that the heat radiation effect can be improved. Since the contact area to the air is increased, an amount of heat of the radiating plate 10, 14, 40 to be radiated into the air is increased, thereby promoting the heat radiation effect.

(TENTH EMBODIMENT)

A semiconductor package according to a 10th embodiment of the present invention will be described with reference to Figs. 11A and 11B.

In the 10th embodiment of the present invention, a plurality of bumps 24 are formed to each of the upper first electrode (upper a electrode) and the upper second electrode (upper b electrode) of the semiconductors 1, 1A, 1B (represented by the semiconductor 1 in the description below and the drawings), and then, pillared or spherical electrodes 11 are joined then to the plurality of bumps 24. The bump 24 is not limited to gold, but may be formed of copper or aluminum. In the gold bump 24, the height stability can be easily ensured. In the copper bump 24, the electrical resistance and the cost can be decreased. In the aluminum bump 24, the processability can be improved.

The plurality of bumps 24 of gold are formed to the upper first electrode (upper a electrode) 2 and the upper second electrode (upper b electrode) 3 of the semiconductor 1 by a bump formation method using general ultrasonic oscillation. The bumps 24 are preferably formed to be scattered as much as possible inside the upper first electrode (upper a electrode) 2 and the upper second electrode (upper b electrode) 3 and in a range not larger than a bottom area of the pillared or spherical electrode 11. If the bumps 24 are formed in an unbalanced state and

concentrated to one side, the pillared or spherical electrode 11 is sometimes inclined at the mount time of the pillared or spherical electrode 11 or a connection area of the pillared or spherical electrode 11 is apt to reduce, leading to a connection failure.

A sectional shape of the bump 24 is not specified. A variation of approximately 10μm in height of the bumps 24 generated when formed is allowed because the bumps are pressed and crushed when the pillared or spherical electrode 11 is mounted. However, for enhancing an effect in height adjustment when the pillared or spherical electrodes 11 are mounted, the bumps are preferably formed as high as possible and no particular problem is brought about when the height is 50μm or more.

According to the above construction, after the plurality of bumps 24 are formed to each of the upper first electrode (upper a electrode) 2 and the upper second electrode (upper b electrode) 3 of the semiconductor 1, the pillared or spherical electrodes 11 are joined onto the bumps 24. As compared with the case where large electrodes, i.e., pillared or spherical electrodes 11 are directly joined to the upper first electrode (upper a electrode) 2 and the upper second electrode (upper b electrode) 3 of the semiconductor 1, the semiconductor 1 is less damaged when the semiconductor 1 has the small gold bumps 24 formed

through ultrasonic oscillation. When the pillared or spherical electrodes 11 are mounted on the bumps 24 through ultrasonic oscillation, the bumps 24 are deformed thereby easing a load to the semiconductor 1 and adjusting the height. The gold bump 24 has a good solderability, enabling joining to the pillared or spherical electrodes 11 by solder.

In each of the above-described embodiments, the lower electrode of the semiconductor 1, 1A, 1B having the electrodes to both of the upper and lower faces is joined with use of the solder to the radiating plate 10, 14, 40, and moreover the pillared or spherical electrodes 11 are joined to the upper electrodes of the semiconductor and the radiating plate. The semiconductor package of a high reliability can be consequently formed easily and stably. More specifically, the electrode at one face of each semiconductor 1, 1A, 1B which has electrodes formed to both faces is directly joined to the radiating plate 10, 14, 40, so that the heat of the semiconductor 1, 1A, 1B can be quickly absorbed and diffused, with the heat radiation effect improved. At the same time, since the pillared or spherical electrodes 11 thicker than a wire used in wire bonding and a larger current capacity than the wire are employed for the connection, the pillared or spherical electrodes 11 can be utilized as connecting terminals to the circuit board.

In the case of the insulating ceramic radiating plate 14, 40, having insulating function, semiconductors 1A and 1B of different functions can be mounted simultaneously.

The present invention is not limited to the foregoing embodiments and can be executed in other various modes.

For example, each of the above embodiments is primarily related to the case where one semiconductor 1 is mounted on the metallic or ceramic radiating plate 10, 14, 40. If a plurality of semiconductors of the same kind are mounted or a plurality of semiconductors 1A and 1B of different types are mounted, a circuit of a wide range can be formed small with a higher efficiency than when one semiconductor 1 is mounted. If the plurality of semiconductors are mounted, wiring between the semiconductor elements, i.e., ICs becomes short to lower an impedance, whereby an electric high frequency transmission loss is reduced and an efficiency can be improved. When an electronic circuit module used in combination of a predetermined plurality of ICs is incorporated in one package, a ratio of a dead space decreases and the dead space becomes small. In other words, for example, in the case where two kinds of semiconductors for a transistor and for a diode are to be used, the semiconductors pair in terms of an electronic circuit are to be used, and therefore leads

of the above one package can be reduced to three although the semiconductors in different packages need five leads. The circuit of a large range can accordingly be formed small.

One example where the semiconductor package of the embodiment is applied to actual products, are power modules such as motors for industrial use, such as AC servo motors, usable for robots or component mounting apparatus. Specifically, such a motor has the motor output of 100-200W, the normal calorific value of 10-20W, the load or abnormal calorific value of 20-100W or 20-200W, performing a switching conversion function of a semiconductor element at normal time and an accelerating and decelerating motion at loading time, and causing a locking motion of motor's rotary shaft at abnormal time. In this case, each electrode has the following outer diameter and height: 1mm-diameter of each electrode at the substrate side and the semiconductor element side, 1mm-height at the substrate side, and 0.5mm-height at the semiconductor side. The shape of each electrode is column. The load voltage of the semiconductor element is 200V, and the current is 1-5A. Taking into account with insulating properties, a distance between the adjacent electrodes having different potentials is away from each other by at least 0.4mm and the electrodes are preferably coated with an insulating resin.

As above, according to the present invention, the

lower face electrodes of semiconductors each having electrodes formed to both upper and lower faces are joined with use of the solder to the radiating plate, and moreover, pillared or spherical electrodes are joined to the upper face electrodes of the semiconductor and the radiating plate. The semiconductor package constituted with use of one or a plurality of semiconductors can be formed in a simple structure with a superior heat radiation effect and a stable quality.

Concretely, since the lower electrodes of the semiconductors are joined to the radiating plate, the heat generated at the semiconductors can be directly transmitted to the radiating plate. Moreover, the upper first electrode (upper a electrode) and the upper second electrode (upper b electrode) of the semiconductor are joined to the radiating plate with use of the pillared or spherical electrodes which are thicker than a gold or aluminum wire used for wire bonding and hard to deform after the joining. The other ends of the pillared (columnar) or spherical electrodes can be utilized as connecting parts to the circuit board. Accordingly, the present invention provides the semiconductor package which can cope with a large current, can easily improve the heat radiation efficiency and secure a distance between electrodes. The semiconductor of a large operating current and voltage and a large heat amount can be

mounted compact, inexpensively and highly reliably and can be manufactured stably.

When the semiconductor and the face of the radiating plate joined to the semiconductor are covered with the sealing resin in a manner to expose part of leading ends of the pillared or spherical electrodes, each component can be protected from deformation, damage, moisture, dust, and the like and becomes easy to handle with as a semiconductor package after completed.

When independent electric circuits of a plurality of polarities of a single or combination of gold, silver, copper, nickel, and tungsten are arranged to the ceramic of the radiating plate and semiconductors of different kinds are joined to the electric circuits of the plurality of polarities of the radiating plate, the independent plurality of polarities can be formed independently of each other on the same face of the radiating plate 14 with the utilization of insulating properties, heat conduction, and heat radiation properties of the ceramic.

When the radiating plate is formed in a multi layer structure of ceramic having semiconductors and electrodes for the pillared or spherical electrodes formed of a single or combination of gold, silver, copper, nickel, and tungsten to the front face thereof and also having the conductor layers formed of the same material as the material

of the electrodes of the front face between the ceramic layers to be connected to the electrodes of the front face to radiate heat from both the ceramic radiating plate and the conductor layers, the heat generated at the semiconductors can be transmitted from the electric circuits through the conductor layers and internal conductors to the lower ceramic plate with utilization of heat conduction properties of the metal. Accordingly, a heat diffusion efficiency is improved and a heat radiation efficiency can be made much better.

In the case where one semiconductor is to be mounted or a plurality of semiconductors having lower electrodes of an equal current and voltage characteristics are to be mounted, the radiating plate itself can be a conductor. If the radiating plate is formed of any one of copper, copper alloy, aluminum, and aluminum alloy, or the radiating plate is formed of the metal after subjected to a surface treatment, the material forming the radiating plate transmits heat and electricity good, diffuses heat quickly and is easy to solder among metals, so that the heat radiation effect for the semiconductors can further be effectuated.

When part of the sealing resin and part of the pillared or spherical electrodes are removed simultaneously after the pillared or spherical electrodes are covered with

the sealing resin, thereby exposing the electrode parts to form the connecting part, the pillared or spherical electrodes can be uniformed in height accurately.

When the pillared or spherical electrodes are pressed to be smooth after joined to the semiconductors and the metallic radiating plate or sealed with the sealing resin, the pillared or spherical electrodes are deformed to be uniform in height easily when pressured with use of a jig having a smooth face or a mold having a smooth face.

In the case where the pillared or spherical electrodes are formed in the double structure of the hard inside and soft outside, or in the double structure having the outside of a material of a lower melting temperature than the inside, although the soft outside of the pillared or spherical electrodes is deformed when joined to the circuit board, the pillared or spherical electrodes are prevented from being deformed large as a whole because of being supported by the hard inside material, whereby a smoothness can be secured at the leading end parts of the pillared or spherical electrodes.

If the radiating plate is provided with the pits and projections to the front face of the face opposite to the joined face to the semiconductors, the radiating plate has a larger surface area, thus improving the heat radiation effect and, also increasing the contact area to the air,

increasing an amount of heat of the radiating plate for radiating to the air. The heat radiation effect can be promoted.

In an arrangement in which the plurality of bumps are arranged to each of the upper first electrode (upper a electrode) and the upper second electrode (upper b electrode) of the semiconductor, with the pillared or spherical electrodes being joined on the bumps, the semiconductor can be less damaged because the small gold bumps are formed through ultrasonic oscillation than when the large pillared or spherical electrodes are directly joined to the upper first electrode (upper a electrode) and the upper second electrode (upper b electrode) of the semiconductor. Setting the pillared or spherical electrodes on the bumps through ultrasonic oscillation can ease a load to the semiconductor because of the deformation of the bumps and can adjust the height. The gold bump is good in solderability, enabling joining to the pillared or spherical electrodes by a solder.

Although the present invention has been fully described in connection with the preferred embodiments thereof with reference to the accompanying drawings, it is to be noted that various changes and modifications are apparent to those skilled in the art. Such changes and modifications are to be understood as included within the

scope of the present invention as defined by the appended claims unless they depart therefrom.

WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a first semiconductor having electrodes formed to both of an upper and a lower faces;

a heat radiating plate to which a lower face electrode of the first semiconductor is joined with use of a joining member; and

pillared or spherical electrodes which are joined to the upper face electrodes of the first semiconductor and the heat radiating plate respectively.

2. A semiconductor package according to Claim 1, further comprising a sealing resin with which the first semiconductor and a face of the heat radiating plate joined to the first semiconductor are covered in a manner to expose a part of leading ends of the pillared or spherical electrodes.

3. A semiconductor package according to Claim 1, further comprising a second semiconductor having electrodes formed to both of an upper and a lower faces and of the same kind of the first semiconductor, a lower face electrode of the second semiconductor being joined to the heat radiating plate with use of a joining member, the heat radiating plate having an electric circuit of an equal polarity formed of a single or a combination material of gold, silver, copper, nickel, and tungsten and set to ceramic, with the first and

second semiconductors being joined to the electric circuit of the equal polarity.

4. A semiconductor package according to Claim 1, further comprising a third semiconductor having electrodes formed to both of an upper and a lower faces and of a different kind of the first semiconductor, a lower face electrode of the third semiconductor being joined to the heat radiating plate with use of a joining member, the heat radiating plate having an electric circuit of a plurality of polarities independently with the circuit being formed of a single or a combination material of gold, silver, copper, nickel, and tungsten and set to ceramic and with the first and third semiconductors of the different kinds being joined respectively to the plurality of polarities of the electric circuit.

5. A semiconductor package according to Claim 1, wherein the heat radiating plate is constituted of ceramic in a multilayer structure, having a circuit for the semiconductor and the pillared or spherical electrodes with the circuit being formed of a single or a combination material of gold, silver, copper, nickel, and tungsten and set to a front face thereof, and the heat radiating plate has conductor layers formed of an equal material to a material of the electrodes of the front face thereof and arranged between layers of the ceramic to be connected to

the circuit of the front face, so that heat of the semiconductor is radiated by both the ceramic and the conductor layers.

6. A semiconductor package according to Claim 1, wherein the heat radiating plate is formed of any one material of copper, copper alloy, aluminum, and aluminum alloy, or any one of the metals subjected to surface treatment.

7. A semiconductor package according to Claim 1, wherein a sealing resin and the pillared or spherical electrodes are formed by removing simultaneously part of the sealing resin and part of the pillared or spherical electrodes after the pillared or spherical electrodes are covered with the sealing resin, thereby exposing the pillared or spherical electrodes to constitute electric connecting parts.

8. A semiconductor package according to Claim 1, wherein the pillared or spherical electrodes have leading ends pressed smoothly to a uniform height.

9. A semiconductor package according to Claim 1, wherein the pillared or spherical electrode is formed of materials of different hardnesses between an inside thereof and an outside thereof.

10. A semiconductor package according to Claim 1, wherein the pillared or spherical electrode is formed of

materials of different melting temperatures between an inside thereof and an outside thereof.

11. A semiconductor package according to Claim 1, wherein further comprising a fourth semiconductor having electrodes formed to both of an upper and a lower faces and of a different kind of the first semiconductor and having a lower face electrode of an equal current and voltage characteristics to the first semiconductor, the lower face electrode of the fourth semiconductor being joined to the heat radiating plate with use of a joining member, the first and fourth semiconductors are mounted on the heat radiating plate.

12. A semiconductor package according to Claim 1, wherein the heat radiating plate is provided with pits and projections to a front face of a face opposite to a face joined to the semiconductors.

13. A semiconductor package according to Claim 1, wherein a plurality of bumps are disposed between the upper face electrodes of the semiconductor and the pillared or spherical electrodes.

14. A method for forming a semiconductor package, comprising:

joining a lower face electrode of a first semiconductor which has electrodes formed to both of an upper and a lower faces to a heat radiating plate with use

of a joining member; and

joining pillared or spherical electrodes to the upper face electrodes of the first semiconductor and the heat radiating plate respectively.

15. A method for forming a semiconductor package according to Claim 14, further comprising, after the pillared or spherical electrodes are respectively joined to the upper face electrodes of the first semiconductor and the heat radiating plate, covering the first semiconductor and a face of the heat radiating plate joined to the first semiconductor with a sealing resin in a manner to expose a part of leading ends of the pillared or spherical electrodes.

16. A method for forming a semiconductor package according to Claim 14, wherein when the first semiconductor is joined to the heat radiating plate, a lower face electrode of a second semiconductor of the same kind of the first semiconductor which has electrodes formed to both of an upper and a lower faces is joined to the heat radiating plate with use of a joining member and the first and second semiconductors are joined to an electric circuit of an equal polarity of the heat radiating plate with the electric circuit of the equal polarity being formed of a single or a combination material of gold, silver, copper, nickel, and tungsten and set to ceramic.

17. A method for forming a semiconductor package

according to Claim 14, wherein when the first semiconductor is joined to the heat radiating plate, a lower face electrode of a third semiconductor of a different kind of the first semiconductor which has electrodes formed to both of an upper and a lower faces is joined to the heat radiating plate with use of a joining member and the first and third semiconductors are joined to an electric circuit of a plurality of polarities independently of the heat radiating plate with the electric circuit being formed of a single or a combination material of gold, silver, copper, nickel, and tungsten and set to ceramic.

18. A method for forming a semiconductor package according to Claim 14, further comprising, before the semiconductor is joined to the heat radiating plate, forming, on a front face of the heat radiating plate constituted of ceramic in a layer structure, a circuit for the semiconductors and the pillared or spherical electrodes by a single or a combination material of gold, silver, copper, nickel, and tungsten, and arranging conductor layers of an equal material to a material of the electrodes of the front face between layers of the ceramic to be connected to the circuits of the front face thereof, so that heat of the semiconductors is radiated by both the ceramic and the conductor layers.

19. A method for forming a semiconductor package

according to Claim 14, wherein, before the semiconductor is joined to the heat radiating plate, forming the heat radiating plate by any one material of copper, copper alloy, aluminum, and aluminum alloy, or any one of the metals subjected to surface treatment.

20. A method for forming a semiconductor package according to Claim 14, further comprising:

after the pillared or spherical electrodes are respectively joined to the upper face electrodes of the first semiconductor and the heat radiating plate, covering the pillared or spherical electrodes with the sealing resin; and

thereafter removing part of the sealing resin and part of the pillared or spherical electrodes simultaneously, thereby exposing the pillared or spherical electrodes to constitute electric connecting parts.

21. A method for forming a semiconductor package according to Claim 14, further comprising, after the pillared or spherical electrodes are respectively joined to the upper face electrodes of the first semiconductor and the heat radiating plate, pressing smoothly leading ends of the pillared or spherical electrodes to a uniform height.

22. A method for forming a semiconductor package according to Claim 14, wherein when the pillared or spherical electrodes are respectively joined to the upper

face electrodes of the first semiconductor and the heat radiating plate, the pillared or spherical electrode formed of materials of different hardnesses between an inside thereof and an outside thereof is used.

23. A method for forming a semiconductor package according to Claim 14, wherein when the pillared or spherical electrodes are respectively joined to the upper face electrodes of the first semiconductor and the heat radiating plate, the pillared or spherical electrode formed of materials of different melting temperatures between an inside thereof and an outside thereof is used.

24. A method for forming a semiconductor package according to Claim 14, wherein when the first semiconductor is joined to the heat radiating plate, a lower face electrode of a fourth semiconductor having electrodes formed to both of an upper and a lower faces and of a different kind of the first semiconductor and having the lower face electrode of an equal current and voltage characteristics to the first semiconductor, is joined to the heat radiating plate with use of a joining member, so that the first and fourth semiconductors are mounted on the heat radiating plate.

25. A method for forming a semiconductor package according to Claim 14, further comprising providing the heat radiating plate with pits and projections at a front face of

a face opposite to the face joined to the semiconductors.

26. A method for forming a semiconductor package according to Claim 14, further comprising forming a plurality of bumps to the upper electrodes of the semiconductors,

wherein when the pillared or spherical electrodes are joined to the upper face electrodes of the semiconductor, the pillared or spherical electrodes are joined to the upper face electrodes of the semiconductor via the plurality of bumps.

ABSTRACT OF THE DISCLOSURE

Electrodes of one face of a semiconductor which has electrodes formed to both faces and a heat radiating plate are directly joined to quickly absorb and diffuse heat of the semiconductor, thereby improving a heat radiation effect. At the same time, electrodes are connected with use of a wire thicker than a wire for wire bonding and larger in current capacity and can accordingly be utilized as a connecting terminal to a circuit board. Ceramic is used for the heat radiating plate, so that semiconductors of different functions can be mounted simultaneously.

Fig. 1

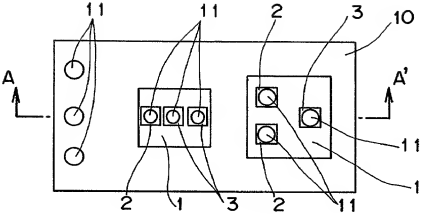


Fig. 2

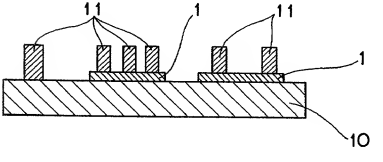


Fig. 3

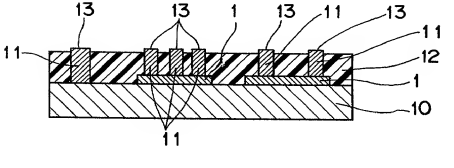


Fig. 4

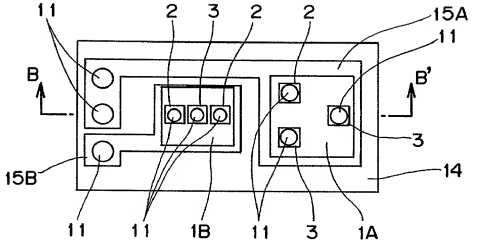


Fig. 5

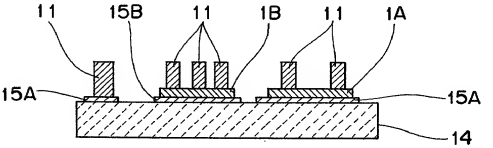


Fig. 6

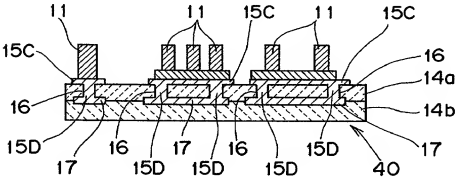


Fig. 7A

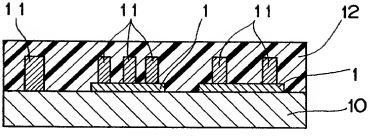


Fig. 7B

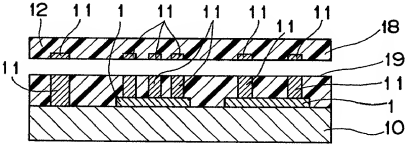


Fig. 8A

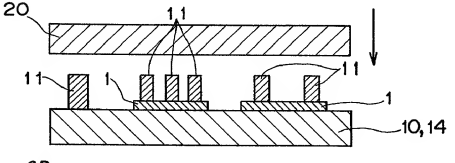


Fig. 8B

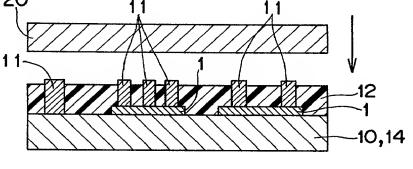


Fig. 9A

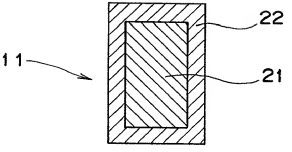


Fig. 9B

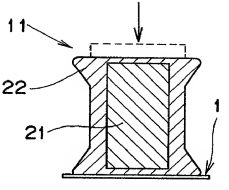


Fig. 9C

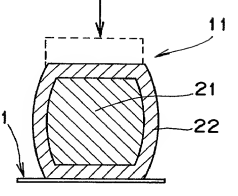


Fig. 10

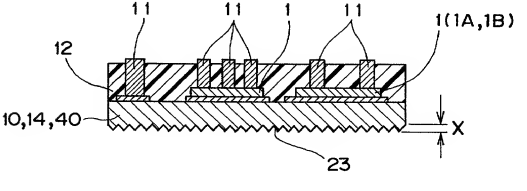


Fig. 11A

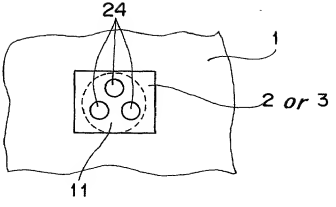


Fig. 11B

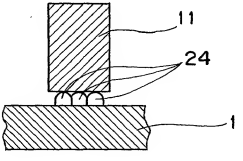


Fig. 12

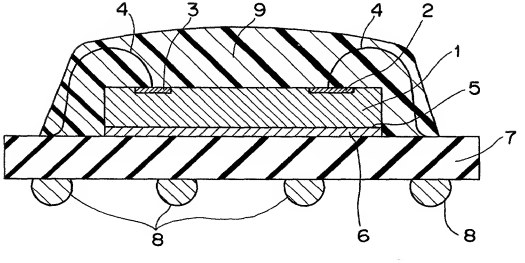


Fig. 13

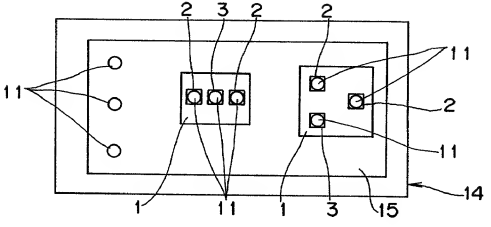


Fig. 14

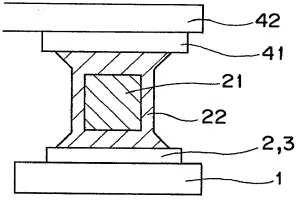


Fig. 15

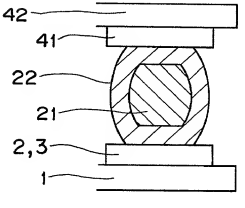


Fig. 16

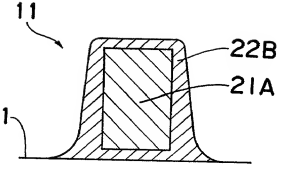


Fig. 17

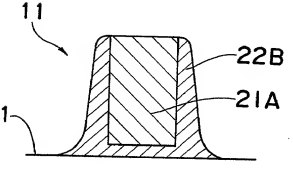
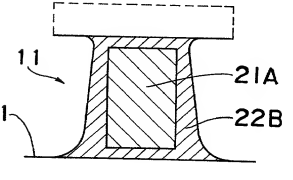


Fig. 18



THE COMMISSIONER IS AUTHORIZED TO CHARGE ANY DEFICIENCY IN THE FEES FOR THIS PAPER TO DEPOSIT ACCOUNT NO. 23-0975

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	
Kazuhiro NOBORI et al.	:	**Attn: APPLICATION BRANCH**
Serial No. NEW	:	Docket No. 2000_1645A
Filed November 28, 2000	:	

SEMICONDUCTOR PACKAGE AND METHOD FOR FORMING SEMICONDUCTOR PACKAGE

COVER LETTER FOR APPLICATION FILED WITHOUT EXECUTED DECLARATION

Assistant Commissioner for Patents,
Washington, DC 20231

Sir:

The above-identified application has been submitted without an executed oath or declaration pursuant to 37 CFR 1.41(c).

It is respectfully requested that this application be assigned a serial number and awarded a filing date pursuant to 37 CFR 1.53.

A duly executed oath or declaration pursuant to 37 CFR 1.63 will be submitted after notification by the U.S. Patent and Trademark Office pursuant to 37 CFR 1.52(d).

A non-executed copy of the Declaration and Power of Attorney, containing the inventorship information, is attached. It is respectfully requested that all communications be directed to the firm indicated on the attached Declaration and Power of Attorney, namely:

WENDEROTH, LIND & PONACK, L.L.P.
2033 K Street, N.W., Suite 800
Washington, D.C. 20006

The required U.S. Patent and Trademark Office Filing Fee is submitted herewith.

Respectfully submitted,

Kazuhiro NOBORI et al.

By ____________________
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November 28, 2000

DECLARATION AND POWER OF ATTORNEY FOR U.S. PATENT APPLICATION

(X) Original () Supplemental () Substitute () PCT () DESIGN

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Title: SEMICONDUCTOR PACKAGE AND METHOD FOR FORMING SEMICONDUCTOR PACKAGE

of which is described and claimed in:
() the attached specification, or
(X) the specification in application Serial No. _____, filed November 28, 2000, and with amendments through _____ (if applicable), or
() the specification in International Application No. _____, filed _____, and as amended on _____ (if applicable).

I hereby state that I have reviewed and understand the content of the above-identified specification, including the claims, as amended by any amendment(s) referred to above.

I acknowledge my duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim priority benefits under Title 35, United States Code, §119 (and §172 if this application is for a Design) of any application(s) for patent or inventor's certificate listed below and have also identified below any application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NO.	DATE OF FILING	PRIORITY CLAIMED
Japan	11-337785	November 29, 1999	YES

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NO.	U.S. FILING DATE	STATUS: PATENTED, PENDING, ABANDONED

And I hereby appoint Michael R. Davis, Reg. No. 25,134; Matthew M. Jacob, Reg. No. 25,154; Jeffrey Nolton, Reg. No. 25,408; Warren M. Cheek, Jr., Reg. No. 33,367; Nils Pedersen, Reg. No. 33,145; and Charles R. Watts, Reg. No. 33,142, who together constitute the firm of WENDEROTH, LIND & PONACK, L.L.P., jointly and severally, attorneys to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith.

I hereby authorize the U.S. attorneys named herein to accept and follow instructions from AOYAMA & PARTNERS as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the U.S. attorneys and myself. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys named herein will be so notified by me.

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Full Name of Fourth Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME	
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP	
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE
Full Name of Fifth Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME	
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP	
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE
Full Name of Sixth Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME	
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP	
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE

I further declare that all statements made herein of my own knowledge are true, and that all statements on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

1st Inventor _____ Date _____
Kazuhiro NOBORI

2nd Inventor _____ Date _____
Yosinori SAKAI

3rd Inventor _____ Date _____
Kazuo ARISUE

4th Inventor _____ Date _____

5th Inventor _____ Date _____

6th Inventor _____ Date _____

The above application may be more particularly identified as follows:

U.S. Application Serial No. _____ Filing Date November 28, 2000

Applicant Reference Number 531900 Atty Docket No. 2000_1645A

Title of Invention SEMICONDUCTOR PACKAGE AND METHOD FOR FORMING SEMICONDUCTOR PACKAGE